Hybrid Switching Amplifier Using a Novel Two-Quadrant Wideband Buffer for Dynamic Power Supply Applications

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Abstract—A hybrid switching amplifier for dynamic power supply applications is presented. To achieve both high speed and high efficiency, a wideband buffered linear amplifier is combined with a hysteresis controlled switching amplifier. To obtain high linearity and reduce switching loss at low power levels where the switching amplifier is not needed, the linear amplifier supplies all load current with the switching one disabled. The novel two-quadrant linear amplifier as a voltage source for regulating the output voltage has a very low output impedance of about 200mΩ around the switching frequency, a high current-driving capability of maximum 220mA and a bandwidth wider than 7MHz. The hybrid amplifier can drive a circuit with an equivalent impedance of 7Ω and supply a maximum output power of 1.1W with a maximum efficiency of about 91%. Its output voltage ranges from 0.3V to 2.9V for a 3.3V supply. The chip is fabricated using only thick-oxide devices in a 0.13um CMOS process and occupies an area of 3.9mm².

I. INTRODUCTION
Spectral efficiency and power efficiency are the most significant issues in recent wireless communication systems. Accordingly, modern or next generation systems (2.5G and 3G) like EDGE, WCDMA, CDMA2000, and WLAN utilize complex modulation techniques to make optimum use of the available spectral bandwidth. Unfortunately, however, the higher spectral efficiency of complex modulation requires envelope variation of the phase modulated RF carrier, which leads to an inherent tradeoff between linearity and power efficiency in traditional transmitter architectures.

This problem has been thoroughly investigated over many years to improve the efficiency with high linearity and many techniques including gate dynamic biasing [1, 2], envelope tracking [3, 4], envelope elimination and restoration (EER) [5, 6] and polar modulation [7-9] have been explored. In particular, EER or polar modulation schemes shown in Fig. 1 have significant potential for power savings in wireless transmitters in that such a tradeoff does not exist because nonlinear power amplifiers are allowed to improve the power efficiency while maintaining the linearity. However, they place very stringent demands on the supply regulation systems because their amplitude and phase components have much wider bandwidths than the original I/Q components. This is why wideband low-dropout linear amplifiers have been still used in the amplitude path in spite of their low efficiencies.

Recently, these linear amplifiers have been replaced by

![Fig. 1. Block diagram of a polar transmitter](image-url)
switching ones for higher efficiency. To increase the bandwidth of switching amplifier, several control methods like interleaving delta modulation (IDM) [9] or hybrid switching technique [10, 11] have been introduced and expensive high-speed processes such as GaAs or SiGe have often been used [3, 4, 6]. CMOS switching amplifier based on IDM concept dissipates considerable power and requires many external components like binary-weighted inductors. Although it is demonstrated in [11] that switching amplifiers using hybrid switching technique which has been suggested for audio applications [12-14] are suitable for high-speed and high-efficiency dynamic power supplies with fewer external components, it is still difficult to design the linear amplifier with wide bandwidth, low output impedance and high current-driving capability [11]. In particular, at low power levels, unnecessary switching results in switching loss, nonlinearity and electromagnetic interference (EMI). In this paper, therefore, a novel hybrid switching technique turning off the switching amplifier at low power levels is introduced and a new buffer amplifier simpler than that in [11] is proposed for two-quadrant operation.

II. HYBRID SWITCHING TECHNIQUE TO IMPROVE THE EFFICIENCY AT LIGHT LOADS

A. Concept of the Hybrid Switching Technique

Fig. 2(a) shows the conceptual diagram of the hybrid switching structure where the linear stage regulates the output voltage as a voltage source and the switching one supplies most of the output current as a dependent current source controlled by the output current of the former (i_L) [11-14]. In other words, the current loop defined as β (≡ i_L / i_a) drives the switching amplifier so that the output current of the linear amplifier is as small as possible. Driving the linear amplifier’s output current as small as possible can be viewed as raising the load impedance seen by the linear amplifier. Because the current loop gain is β, the equivalent load impedance of the linear amplifier is increased by the factor of (1 + β).

The block diagram of a conventional hybrid switching amplifier based on the hysteresis control is shown in Fig. 2(b). If the magnitude of hysteresis window is W as shown in the figure, the output current of the linear amplifier, that is, the inverse of the ripple current is limited to the hysteresis level. Assuming that the input voltage varies slowly compared to the switching period and the output voltage (V_o) can be treated as constant within the switching interval (T), the switching frequency (f_s) can be found as follows:

\[ f_s = \frac{4D \cdot (1 - D)}{f_{s,\text{max}}} \cdot f_{s,\text{max}} \]  

\[ f_{s,\text{max}} = \frac{V_{\text{dd}}}{4L \cdot \Delta i} \cdot \frac{V_{\text{dd}} \cdot A_i}{4LW} \]  

where D is the duty ratio, \( f_{s,\text{max}} \) is the maximum switching frequency, \( A_i \) is the current sense gain and \( \Delta i \) is the peak-to-peak ripple current. Note that the switching frequency will not be fixed because of its dependence on the output voltage.

Because the hybrid switching technique ensures that the linear amplifier usually operates at a much smaller power level than the switching amplifier, it is not difficult to improve the overall linearity of the hybrid switching amplifier through the linear amplifier with higher performance. However, unnecessary switching operation at low power levels where the linear amplifier can drive the output current deteriorates the performance of the overall system including the efficiency, linearity, noise and so on. Reference [14], therefore, proposed a novel control approach of a dead-band at low power levels where the switching amplifier does not assist, allowing the linear amplifier to supply the load without interference, ensuring high fidelity for audio applications.

B. Proposed Hybrid Switching Amplifier

The switching stage of the hybrid switching audio amplifier proposed in [14] consists of two separate buck converters to avoid shoot-through currents and poor reverse recovery characteristics. It also includes a freewheeling circuit to prevent unwanted oscillations. As shown in Fig. 3(b), if the sensed value (\( V_{\text{SEN}} \)) exceeds the upper limit (V_TH) of the hysteresis band, the switching stage begins to supply the output current and then the output current of the linear amplifier (i_a) decreases towards the lower limit (V_TL). In the instant of touching the lower limit, the inductor current (i_L) freewheels through the power MOS to decrease and i_a increases again. The switching operation goes on repeatedly within the hysteresis band so long as the output current does not go under the predefined value. Once the output current decreases less than the predefined value, the direction of i_L changes after a while and then the enable signal (EN) becomes low to turn NMOS switch off. Meanwhile, the output of SR latch (Q) keeps low and the
capacitor $C_I$ in the freewheeling circuit charges towards $V_C$. After the predefined time of $t_F$, the switch $SW_1$ turns on and the residual current of the inductor freewheels through $SW_1$ to disappear. Because the switching node ($V_x$) is floating, only the linear amplifier supplies all the output current. Therefore, switching loss, noise and EMI caused by the needless switching operation do not exist at low power levels.

Component values in the freewheeling circuit are chosen carefully lest the maximum turn-on time of the NMOS switch during the maximum switching period should exceed the value of $(C_I V_C) / I_T$. Otherwise, $SW_1$ turns on during the switching operation. The maximum switching period can be found from the inverse of equation (1).

### III. NOVEL TWO-QUADRANT WIDEBAND BUFFER AMPLIFIER

To control the output voltage, the linear amplifier supplies some amount of signal current within the predefined value and absorbs the switching ripple current from the switching stage. Because the output ripple
Voltage is generated by the multiplication of the ripple current and the output impedance of the linear amplifier; low output impedance at the switching frequency is requisite for low output ripple voltage [11]. In addition, the linear amplifier should be able to source or sink the ripple current while signal current is provided. It means so-called two-quadrant operation because the current direction of the linear amplifier is always positive.

The composite output stages shown in Fig. 4 can make the output impedance very low with relatively low power dissipation because of reducing the output impedance of the SF by a factor of the loop gain of the local feedback loop [15]. Therefore, by widening the local loop, it is possible to implement the output stage with a wide bandwidth, a high current-driving capability, and a very low output impedance even at a high frequency. However, the composite output stage shown in Fig. 4(a) cannot obtain large negative output swing because of the source follower MPSF. As a result, there is a region unable to operate in the second quadrant. In contrast, the output stage in Fig. 4(b) has this type of region in the first quadrant because of the source follower MNSF.

Fig. 5 shows a composite output stage combining the two structures shown in Fig. 4(a) and (b) for complete two-quadrant operation. Two local loops (MNSF-MP1-MPCS, MPSF-MN1-MPCS) can be found in the middle range of the output voltage. In addition, the rail-to-rail control circuit having the switches SW1 and SW2 is included to prevent the output voltage from being clipped by the SF transistor, namely MNSF or MPSF, near the positive or negative supply rail, respectively. In the concrete, during positive output swings, MNSF is turned off by SW1, and the loop (MPSF-MN1-MPCS) sources or sinks the ripple current to eliminate the output ripple voltage. During negative output swings, MPSF is turned off by SW2, and the loop (MNSF-MP1-MPCS) performs the same function.

The complete two-quadrant linear amplifier with wide bandwidth, low output impedance and high current-driving capability is shown in Fig. 6. This is much simpler structure than the four-quadrant amplifier suggested in [11]. Class-AB bias circuit is also unnecessary since the output stage does not require a push-pull structure. Biving of push-pull source followers, MPSF and MNSF, is easily achieved by two diode-connected transistors, MPD and MND. In spite of the diode-connected transistors, the output voltage swing of two-stage OTA is guaranteed by connecting the gates of MNA and MNB each other [16].

**IV. EXPERIMENTAL RESULTS**

Fig. 7 shows a micrograph of the prototype fabricated using thick-oxide devices in 0.13um CMOS process with an area of 3.9mm². The closed-loop gain of the hybrid switching amplifier is 2 and the hysteresis band approximately ranges from 0.6V to 1.4V. Waveforms for a 50kHz sinusoidal and square-wave signal with a 7Ω load are given in Fig. 8 and Fig. 9. Vreset is the reset signal of SR latch, that is, $V_{g}$ and the dotted circle shows the turn-off of the switching stage at low power levels. Fig. 10 shows that the small-signal closed-loop bandwidth is about 7MHz. The simulation result shown in Fig. 11 demonstrates that the output impedance of the linear amplifier is less than 200mΩ at the switching frequency. Fig. 12 shows the efficiency in relation to the output voltage and the load condition. The amplifier can provide a maximum power of 1.1W to a 7Ω load and it has a maximum efficiency of 91% at a 10Ω load. Table I summarizes the measured performance with a 4uH inductor. The ripple current more than about 100mApp can
be reduced to 40mA by a 3rd-order filter and current feedback [11]. Although the linear amplifier was designed to drive 220mA, unfortunately, its current-driving capability was reduced to 40mA at the maximum output voltage due to the channel-length modulation of the output PMOS transistor. This is why the ripple voltage is visible at the output as shown in Fig. 8 and Fig. 9.

V. CONCLUSION

A CMOS hybrid switching amplitude modulator based on a hysteretic control is proposed to achieve both high efficiency and high speed for dynamic power supply applications. Because the linear amplifier supplies all load current with the switching amplifier disabled at low power levels, the performance of the overall system including the efficiency, linearity, noise and so on is improved. We also propose a novel buffer amplifier with a wide bandwidth, low output impedance, two-quadrant operation, and high current-driving capability.

ACKNOWLEDGMENT

This work was supported by the ERC program of the Korea Science and Engineering Foundation (KOSEF) grant funded by the Korea Ministry of Education, Science and Technology (MEST) (No. R11-2007-045-01004-0).

REFERENCES


Fig. 7. Chip micrograph.

Fig. 8. 50kHz sinusoidal response at 7Ω load.

Fig. 9. 50kHz square-wave response at 7Ω load.

Fig. 10. Magnitude response of hybrid switching amplifier.

Fig. 11. Simulated output impedance of the linear amplifier.

Fig. 12. Measured efficiency at various loads.

**Table I. Measured performance parameters.**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
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<tbody>
<tr>
<td>Supply voltage</td>
<td>3.3 V (only 3.3V devices)</td>
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<tr>
<td>Output voltage range</td>
<td>0.3 V ~ 2.9 V</td>
</tr>
<tr>
<td>Maximum output power (Class-E2)</td>
<td>1.1 W @ 7Ω</td>
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<tr>
<td>Switching frequency</td>
<td>~ 2 MHz</td>
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<tr>
<td>Closed-loop BW (small-signal)</td>
<td>~ 7 MHz</td>
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<tr>
<td>Output ripple voltage (with 3rd-order filter)</td>
<td>&lt; 20 mVpp</td>
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<tr>
<td>Zout of linear amp (by simulation)</td>
<td>&lt; 200 mΩ @ 2MHz</td>
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<tr>
<td>Current driving capability of linear amp</td>
<td>40 mA ~ 220 mA (w.r.t. Vout)</td>
</tr>
<tr>
<td>Maximum efficiency</td>
<td>~ 91% @ 10Ω</td>
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